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ARTICLE

Electron-Transparent Thermoelectric Coolers Demonstrated with Nanoparticle and Condensation Thermometry

William A. Hubbard,[‖] Matthew Mecklenburg,[‖] Jared J. Lodico,[‖] Yueyun Chen, Xin Yi Ling, Roshni Patil, W. Andrew Kessel, Graydon J. K. Flatt, Ho Leung Chan, Bozo Vareskic, Gurleen Bal, Brian Zutter, and B. C. Regan*

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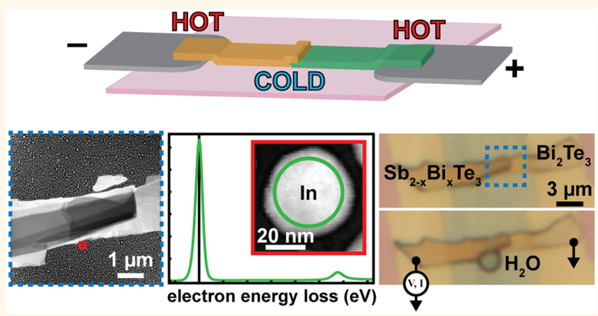
ABSTRACT: **More efficient thermoelectric devices would revolutionize refrigeration and energy production, and low-dimensional thermoelectric materials are predicted to be more efficient than their bulk counterparts. But nanoscale thermoelectric devices generate thermal gradients on length scales that are too small to resolve with traditional thermometry methods. Here we fabricate, using single-crystal bismuth telluride (Bi_2Te_3) and antimony/bismuth telluride ($Sb_{2-x}Bi_xTe_3$) flakes exfoliated from commercially available bulk materials, functional thermoelectric coolers (TECs) that are only 100 nm thick. These devices are the smallest TECs ever demonstrated by a factor of 10^4. After depositing indium nanoparticles to serve as nanothermometers, we measure the heating and cooling produced by the devices with plasmon energy expansion thermometry (PEET), a high-spatial-resolution, transmission electron microscopy (TEM)-based thermometry technique, demonstrating a $\Delta T = -21 \pm 4$ K from room temperature. We also establish proof-of-concept for condensation thermometry, a quantitative temperature-change mapping technique with a spatial precision of $\lesssim$300 nm.**



KEYWORDS: *thermoelectric, exfoliated, bismuth telluride, STEM, EELS, EBIC, condensation*

While thermoelectric devices are used in niche applications due to advantages such as small size, lack of moving parts, and reliability, their low efficiency compared to conventional, compression-based heat engines has prevented widespread adoption of the technology.[1−3] For maximum device performance, one desires thermoelectric materials with large Seebeck coefficients S, large electrical conductivities σ (to minimize Joule heating), and small thermal conductivities κ (to maintain large thermal gradients). However, identifying materials that have simultaneously favorable S, σ, and κ has proved challenging.[4] To improve on the performance of bulk materials, researchers are therefore exploring strategies such as nanostructuring.[2,5−9] In a two-dimensional (2D) structure, for instance, the effects of electron confinement and phonon boundary scattering might decrease the ratio κ/σ relative to its bulk value.[4,5,10]

Bismuth telluride (Bi_2Te_3) and the related solid solution, antimony−bismuth telluride ($Sb_{2-x}Bi_xTe_3$), are commonly paired in commercially available thermoelectric coolers (TECs), as they have reasonably large S, large σ, and small κ near room temperature.[11,12] Bi_2Te_3 and its alloys are also van der Waals materials that can be mechanically exfoliated into atomically thin single crystals,[13] and single crystals of bismuth telluride exhibit improved thermoelectric properties relative to their polycrystalline counterparts.[14] Thus, Bi_2Te_3 and $Sb_{2-x}Bi_xTe_3$ are ideal candidates for producing a two-dimensional TEC.[15,16]

Evaluating the nanometer-scale thermal gradients that arise in microscale (and smaller) TECs is challenging: optical thermometry techniques have barely sub-micrometer spatial resolution, while scanning probe techniques require specialized, expensive equipment.[17−21] Both of these approaches require

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nontrivial calibrations. We have recently developed a high spatial resolution, noncontact, STEM-based thermometry technique, plasmon energy expansion thermometry (PEET).[22] PEET also requires specialized, expensive equipment, but the expensive item, namely a scanning TEM (STEM) equipped with electron energy-loss spectroscopy (EELS), is general purpose and commonly found at large research institutions. PEET determines temperature *via* measurements of thermal expansion, which is quantified by precise measurements of a bulk plasmon energy. A modern EELS system on a STEM can produce plasmon energy maps with sufficient precision to detect the density variations at atomic-scale features such as grain boundaries.[22] Thus, PEET has the spatial resolution to map thermal gradients at the few nanometer scale, an almost unexplored regime for nanostructured thermoelectric materials. As a step toward such a study, here we apply PEET to achieve point temperature measurements inside the TEM.

Several competitive vacuum TEM-based continuous (*i.e.*, not binary) thermometry techniques are under development. Electron diffraction patterns are also sensitive to thermal expansion and thus can be used to extract the temperature of both crystalline[23,24] and amorphous[25] materials *in situ*. The thermal diffuse scattering of beam electrons by phonons provides a temperature-dependent signal that can be exploited for temperature mapping.[26] High-resolution EELS can quantify phonon occupation numbers in the <100 meV energy regime and, *via* an elegant application of the principle of detailed balance,[27,28] extract temperatures without reference to any external calibration.

Relative to PEET for the thermometry of bismuth telluride thermoelectrics, each of these techniques has advantages in principle. For instance, none requires the addition of a separate thermometric material, as PEET does in this case. At present, however, these techniques are relatively undeveloped. For instance, only one has mapped a temperature gradient (ref 24 with 27 pixels separated by 10s of μm), while PEET has generated maps with tens of thousands of pixels on a 4 nm pitch.[22] Of course, access to the necessary equipment and familiarity with the technique[20,22,29] also heavily influenced the decision to use PEET.

To supplement the PEET measurements, we also introduce condensation thermometry, which requires no uncommon or expensive equipment. If employed in an optical microscope, this technique can locate (to better than the microscope's resolution limit[30]) and quantify (to better than 1 K precision) hot and cold spots on a device. The basic idea is simple: in an atmosphere containing condensable vapor, a sufficiently cold spot on a device's surface will condense some vapor into an optically detectable droplet. Previously, precision temperature measurements have been used to determine condensation coefficients on, for example, the wall of a boiler's condenser.[31] Here we are reversing that logic, using evidence of condensation to determine the temperature. As with a cloud chamber,[32] operating near a vapor-to-liquid phase transition makes an otherwise-invisible phenomenon visible (*i.e.*, the temperature and the trajectory of a high energy particle, respectively).

For our experiments, the ambient air serves as a convenient atmosphere and its concomitant water vapor as the condensable fluid. However, a controlled atmosphere with some other vapor might be employed to reach a different temperature regime or to solve a chemical compatibility problem. Regardless, putting the entire chip at a temperature T_{chip} either right above or right below the condensation temperature T_c (*i.e.*, the vapor-pressure-dependent temperature where the evaporation rate and the condensation rates are equal) allows one to identify cold and hot spots, respectively, as they appear when the device is powered. This technique is thus applicable in those particular circumstances where the device base temperature (here T_{chip}) is adjustable, where temperature gradients can be toggled on and off, and where the system can tolerate fluid exposure. Because the fluid exposure introduces additional thermal mass and conductance that disturb the system temperature, condensation thermometry's errors are minimized (and its spatial precision is best) when the droplet sizes are also minimized.

In the case of water vapor, T_c, known as the "dew point", is the temperature corresponding to 100% humidity (*i.e.*, the atmosphere is saturated with water). For T_{chip} just warmer than T_c, a cold spot will condense a droplet. Conversely, for T_{chip} just cooler than T_c, a hot spot will evaporate an existing droplet. Both T_{chip} and T_c are easily determined using standard thermometers. A hygrometer is also helpful if water is serving as the condensable fluid. Changing T_{chip} while observing the resulting effects on a hot/cold spot droplet (and holding T_c constant) allows one to quantify temperature changes at that spot.

To measure nanoscale device temperatures in an ambient atmosphere, several other techniques could be employed. For instance, thermometry techniques using lanthanide-doped upconverting nanoparticles,[33,34] fluorescent quantum dots,[35] and nitrogen vacancy centers in nanodiamonds[36,37] have excellent spatial resolution and temperature sensitivity. They are also biocompatible and can measure temperature in the absence of a switchable temperature gradient. For electronic devices (particularly TECs), however, condensation thermometry might be preferred for its simplicity and accessibility, as it requires no specialized materials (*e.g.*, nanoparticles) or equipment (*e.g.*, lasers).

RESULTS AND DISCUSSION

We fabricate electron-transparent TECs by exfoliating[13,15,16] single crystals of commercially available *n*-type Bi_2Te_3 and *p*-type $Sb_{2-x}Bi_xTe_3$ material onto silicon chips prepared with electron-transparent windows and platinum electrodes (see Methods). For a side-by-side comparison of our device architecture with the traditional Π-type geometry, including labels showing where cooling and heating occur, see Supporting Figure 1. A completed device (Figure 1) has good overlap at the three junctions made by the two flakes, which are determined with scanning electron microscopy (SEM) to be 60 nm and 90 nm thick for the *p*-type and *n*-type flakes, respectively (Supporting Figure 2; see Supporting Figures 3 and 4 for other measured thicknesses). However, because of the difficulties in arranging clean surfaces during the transfer process, good ohmic contact at the junctions is not guaranteed by such mechanical overlap.[38] But with the device already wired for biasing, the quality of the interfacial connections can be evaluated with electron beam-induced current (EBIC) imaging using methods that we have previously reported.[38]

With the *n*-type flake's side of the TEC circuit grounded (Figure 1a), we use a transimpedance amplifier (TIA) to measure the current produced on the *p*-type flake's side as the STEM beam rasters across the field of view. Associating this current with the beam position generates an EBIC image simultaneously with the standard STEM (*e.g.*, bright field, annular dark field, *etc.*) images. Current is generated when the

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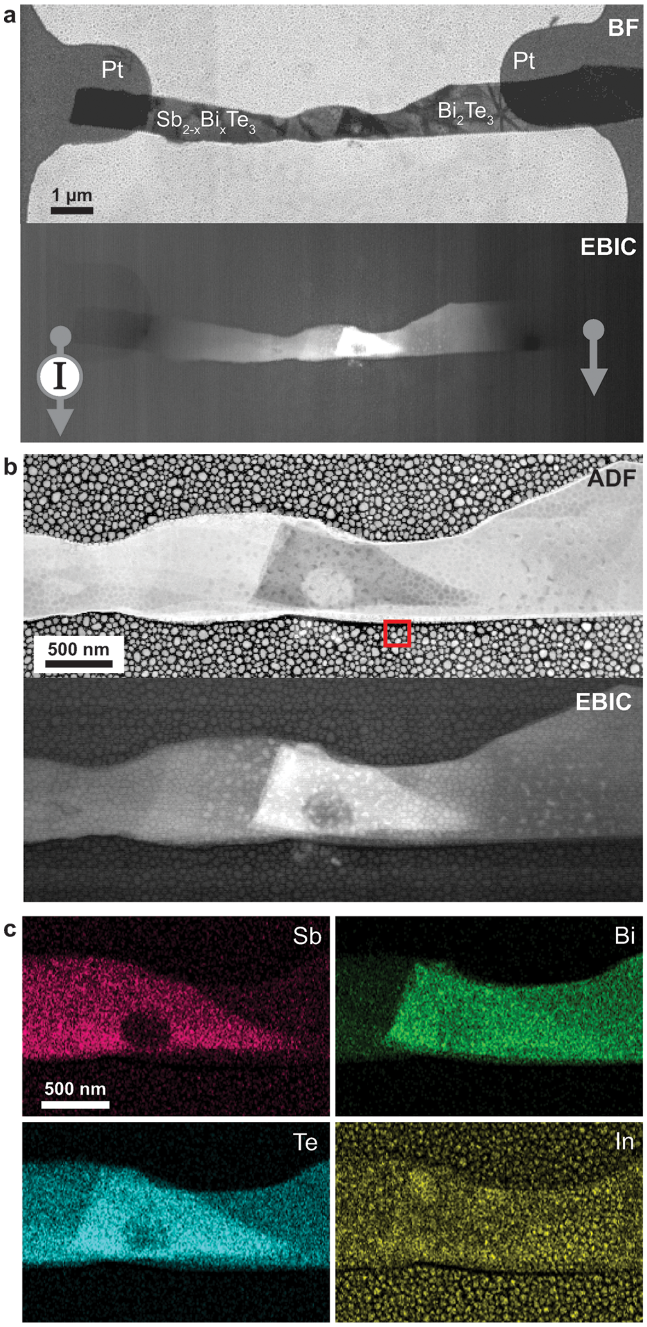

Figure 1. STEM images of a $Bi_2Te_3/Sb_{2-x}Bi_xTe_3$TEC device. (a, top) Low-magnification bright-field (BF) STEM image gives a device overview, showing two semiconductor flakes bridging the gap between platinum electrodes. (b, top) Higher magnification annular dark field (ADF) image of the semiconductor heterojunction shows a nearly uniform but discontinuous film of indium nanoparticles coating the device and the supporting Si_3N_4 membrane. (a and b, bottom) STEM EBIC images acquired simultaneously with the standard STEM images highlight areas with strong electric fields (both polarities are evident in the low-magnification image). The location of the TIA and the nanoparticles chosen as nano-thermometers (red box) are indicated. (c) EDS maps of antimony (Sb), bismuth (Bi), tellurium (Te), and indium (In) show the expected elemental distributions and confirm the extent of the flake overlap indicated by the standard STEM and STEM EBIC imaging.

primary electron beam produces electron−hole pairs in the sample and these pairs are separated by a local electric field. The local electric field might be produced by an externally applied voltage, or by internal charge transfer, such as occurs in a *p*−*n* junction.[39] The positive current at the junction of the two flakes, indicated by bright contrast in the Figure 1 EBIC images, indicates an electric field pointing from the *n*- to the *p*-type flake, as expected. The brighter contrast toward the left of the overlap region indicates a larger electric field and a better connection. We thus expect the most cooling to occur near this bright region. Comparison of the dark-contrast regions where the flakes overlap the Pt electrodes indicates that the *p*-type $Sb_{2-x}Bi_xTe_3$ is making more uniform contact than the *n*-type Bi_2Te_3 and that the electric fields point into the *p*-type and out of the *n*-type flakes at the metal−semiconductor junctions, just as at the semiconductor−semiconductor junction.

Interestingly, an ellipsoidal region with low contrast appears in the standard STEM images (Figure 1a,b, top), the EBIC images (Figures 1a,b, bottom), and some of the channels of the energy-dispersive X-ray spectroscopy (EDS) images (Figure 1c). Relative to the maximum signal, the ellipsoidal region is normal in indium, weak in bismuth, weaker in tellurium, and weakest in antimony. We thus attribute this ellipsoidal feature to a void in the $Sb_{2-x}Bi_xTe_3$ flake.

Having mapped the device's physical layout with standard STEM, SEM, and EDS, and its electrical properties with STEM EBIC, we now evaluate its thermal performance using PEET. With a biasing sample holder (Hummingbird Scientific) and a JEOL JEM-2100F equipped with a Gatan Quantum SE imaging filter, we image at 80 kV, using parameters as described previously.[29] (Reference 29 uses silicon, rather than indium, nanoparticles as nanothermometers.) As we vary the current through the device from −100 to 0 μA in 10 μA steps (see Figure 2 and Supporting Figure 5a), we acquire a series of spectrum images of an indium nanoparticle adjacent to the semiconductor heterojunction. While the nanoparticle is not in direct contact, it is thermally coupled to the heterojunction by the silicon nitride membrane, and it is more easily viewed in transmission than a nanoparticle on the heterojunction itself. Analysis of these spectra gives the nanoparticle's temperature as a function of the TEC device bias (see the Supporting Information).

As the applied TEC bias current decreases from zero, the nanoparticle cools first to a minimum near 0 °C and then warms as the current I is further decreased. This behavior is expected: the TEC functions as a cooler in reverse-bias at low currents because the Peltier effect $\propto I$ dominates, but eventually Joule heating $\propto I^2$ takes over.[40] Fitting the temperature data to a second-order polynomial (Figure 2c, blue) gives the result $\Delta T = (-21 \pm 4\ \mathrm{K})(1 - [1 + I/(56 \pm 2\ \mu\mathrm{A})]^2)$.

This device's size, defined by the volume of its thermoelectric materials, is less than 2 μm^3 (Supporting Figure 2). Peltier cooling effects (*e.g.*, a temperature signal at the same frequency as the applied current) have been reported in similarly sized devices,[21,41−44] but these devices generally have a comparable Joule heating effect (at twice the frequency of the applied current). Devices with one dimension $\lesssim$10 μm showing actual cooling have been reported,[45−48] but in all cases the device volume, even considering the "device" to be only a single *p*−*n* couple, is more than 10^4 times larger. To our knowledge, this demonstration is the first of net steady-state cooling in a thermoelectric device with a nanoscale (*i.e.*, sub-micrometer) spatial dimension.

This device of Figures 1 and 2 thus achieves an optimum $\Delta T_{cool} = -21 \pm 4$ K at a current of -56 ± 2 μA. Of the dozens of

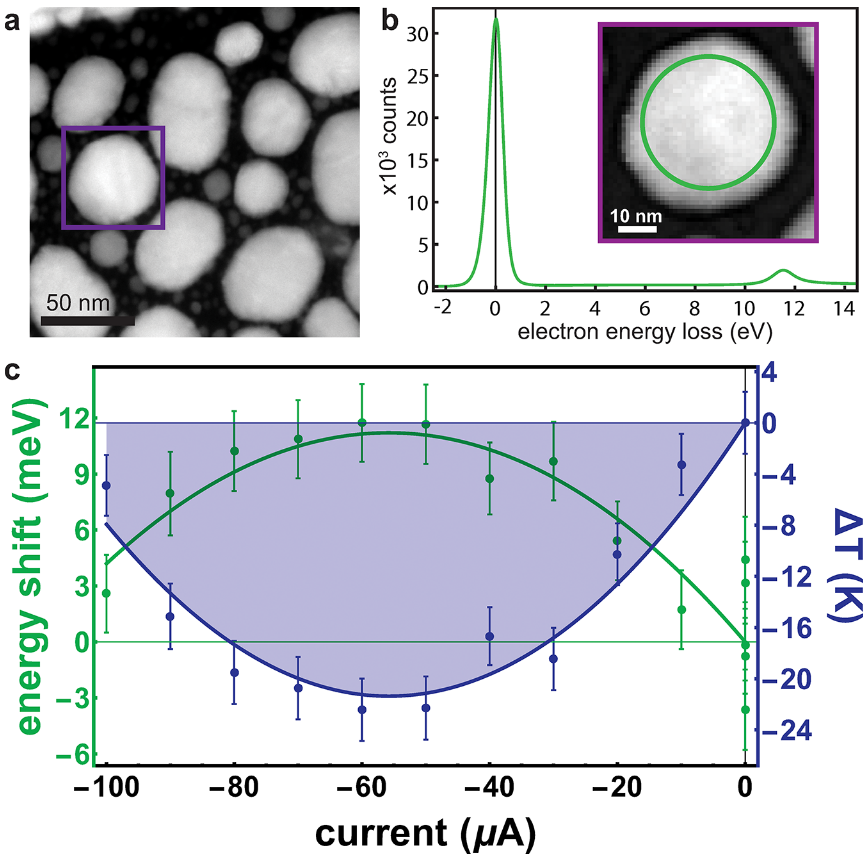

Figure 2. STEM ADF image, EELS spectrum, and cooling curves from an In nanoparticle near the TEC heterojunction. The ADF STEM image (a) shows, at higher magnification, the region highlighted in red in Figure 1b. The edge of a flake can be seen in its upper left corner. An energy slice (b, inset), 1 eV wide and centered on the indium plasmon peak, through a spectrum image shows the intensity of the plasmon signal in the region boxed in purple in the ADF image. Summing the spectra acquired within the circular green region indicated in the inset energy slice gives the low-loss spectrum (b, plot), with the zero-loss peak at 0 eV and the first indium plasmon at 11.5 eV. The indium plasmon peak center (green) and the corresponding temperature (blue), plotted (c) as a function of the applied current, show that maximum cooling (∼21 K) is achieved near −56 μA.

complete devices fabricated (for PEET measurements on other devices, see Supporting Figure 6), this device has one of the lowest total resistances, $R = 3.5$ kΩ at zero bias. (The resistance is measured with a two-wire technique, and thus includes ∼700 Ω of on-chip lead resistance.) For a flake resistivity of $\sim 2 \times 10^{-5}$ Ω·m (determined by measurements on the bulk materials), this total resistance is consistent with little contact resistance.

This device also gives the largest ΔT observed. We find that higher resistance devices generally exhibit correspondingly less cooling, and we attribute high device resistances to poor ohmic contact between the overlapped flakes, or between the flakes and the Ti/Pt electrodes. Device resistance can sometimes be improved by annealing, either in a tube furnace at 120 °C (ref 49) or by direct biasing, with a vacuum environment or inert atmosphere being preferable to air. (Annealing is always performed before indium deposition.) We note also that the devices are sensitive to usage and the ambient atmosphere: an *in situ* STEM experiment with hard biasing might cause the device resistance to improve by an order of magnitude, while sitting on the shelf in air for a month might cause an equally large (but possibly reversible) change in the other direction.

These tiny TEC devices can be tested without PEET (and the EELS-equipped STEM, biasing sample holder, and data analysis that PEET requires) by using condensation thermometry in an optical microscope. We demonstrate both PEET and condensation thermometry on another device (Figure 3) that has the same basic architecture as that of Figures 1 and 2. The device's physical structure, electronic structure, and thermoelectric performance are first evaluated with STEM, STEM EBIC, and PEET respectively (Figure 3a,b). STEM imaging shows that the device's flakes are of nonuniform thickness, while STEM EBIC shows that largest electric fields (and thus the best electrical contact) in the semiconductor heterojunction occur well toward one side. PEET applied to an indium nanoparticle thermometer on the silicon nitride membrane near the best contact region gives a best cooling value of $\Delta T_{cool} = -8 \pm 4$ K at a bias of -78 ± 15 μA in the high vacuum of the TEM (see Supporting Figure 5b). During these PEET experiments the device resistance averaged 2.5 kΩ (which includes the same ∼700 Ω of lead resistance).

Condensation thermometry gives a dynamic and functional perspective of the cooling capabilities of the device. We test in the ambient atmosphere of Los Angeles, which typically has low humidity and thus is noncondensing in the absence of a cooled surface. The test setup consists of a digital hygrometer (ThermoPro TP50), a 30 mm × 30 mm × 4.7 mm Peltier module (Custom Thermoelectric), an adjustable DC power supply, and a K-type thermocouple thermometer. The Peltier module has lapped ceramic (Al_2O_3) faces, is rated for 19 W, and is powered by 31 couples of the same materials used to make the electron-transparent TEC devices discussed in this paper. Mounting a TEC device's chip on the Peltier module (suitably

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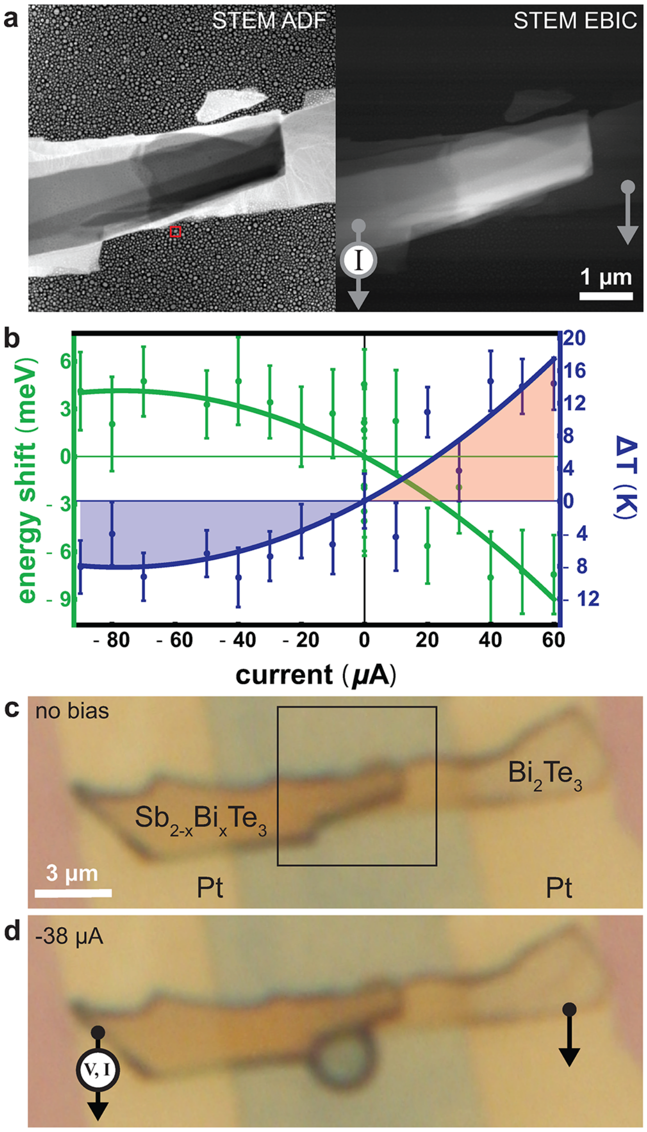

Figure 3. STEM images, PEET-derived cooling curves, and optical condensation thermometry on a single TEC device. (a, left) Standard ADF STEM imaging shows a TEC device's coating of indium nanoparticles, and that the flake thicknesses are not uniform. (a, right) Simultaneous STEM EBIC reveals that the best contact between the flakes is made nearer the lower edge of the heterojunction. (b) PEET on an indium nanothermometer (red box) indicates a cooling of ∼8 K. (c) In air, under an optical microscope, the unbiased TEC device shows no condensation. (d) A −38 μA bias current forms a dewdrop adjacent to the heterojunction, near the "best-contact" region identified with STEM EBIC. The power source labeled "*V, I*" is not to be confused with the EBIC TIA labeled "*I*".

heat-sunk), we measure the temperature of the module's top surface with the thermocouple to find T_{chip}. (The heat leak through the electrical probes that hold down the 2 mm × 2 mm × 200 μm silicon chip and access the TEC, and the ≲15 μW dissipated by the TEC itself, represent a negligible heat load.)

We first demonstrate the gross properties of the TEC cooling curve (Figure 3 and Supporting Movie 1). Setting the Peltier module to produce a T_{chip} = 3.8 °C, we ramp the TEC reverse bias in 10 mV steps. At the smallest bias voltages nothing happens, but a small droplet appears (see Supporting Movie 1) at −60 mV (−18 μA) and continues to grow as the voltage is further decreased. When the voltage reaches −120 mV (−41 μA), however, the droplet begins to shrink, nearly disappearing by −220 mV (−65 μA). Ramping the bias in the other direction shows the expected reversibility with no obvious hysteresis. This droplet growth behavior (*i.e.*, initial growth to a maximum followed by shrinkage and disappearance) is exactly that expected based on the temperature changes observed previously on this device with PEET (*i.e.*, cooling to a minimum followed by warming as a function of increasing reverse bias). Note also that the drop nucleates and grows near the location that is expected, based on the STEM EBIC imaging, to show the most cooling.

Condensation thermometry can also vividly demonstrate the microscale-TEC's speed, and quantify the cooling achieved. Changing the voltage bias in a step from zero to the cooling optimum produces a droplet on a time scale which is effectively instantaneous relative to the video acquisition rate of 2 frames/s (Supporting Movies 1 and 2). For this device's thermal time constant, dimensional analysis gives an estimate $\tau \sim CL^2/\kappa$, which, with a volumetric heat capacity of $C \simeq 1.2 \times 10^6$ J/m^3·K, thermal conductivity $\kappa \simeq 2$ W/m·K, and characteristic length (from the cold spot to the heat sink) $L \simeq 6$ μm, is $\tau \sim 20$ μs. Bringing the voltage bias back to zero causes the droplet to disappear equally quickly.

The ΔT achieved is quantified by increasing T_{chip} away from the dew point T_c, which makes forming a droplet more difficult. Here, with the hygrometer measuring the dew point T_c = 11.8 °C, setting T_{chip} = 18.6 ± 0.5 °C gives a just-visible droplet at the cold spot with I = −37 μA, implying a ΔT_{cool} = −6.8 ± 0.5 K (Supporting Movie 2). The agreement between the mean ΔT_{cool} value determined by PEET and that determined by condensation thermometry is excellent, but may be the result of a fortuitous combination of statistical and systematic shifts. Between the two experiments, the ambient pressure increased, the device resistance increased, and the distance between the cooling site and the thermometer decreased. These changes would tend to decrease, decrease, and increase the size of the cooling effect observed, respectively, as the heat leak to room temperature is exacerbated, the device's cooling efficiency drops, and the droplet is more likely to measure the coldest spot than the chosen nanoparticle. Based on the good agreement we expect that the semiconductor-metal contacts, not the semiconductor−semiconductor contact, are responsible for the resistance increase, as its deleterious effect would be smallest there.

The small droplet limit is preferred for condensation thermometry. Such just-visible droplets minimize the thermal load (and thus the temperature measurement error) while maximizing the spatial precision of the (point) temperature measurement. Sparse objects (*e.g.*, droplets) smaller than the microscope's diffraction limit cannot be resolved, but their centers can be localized to a precision about an order of magnitude greater than the microscope resolution.[30] A microscope such as ours, equipped with a high-quality objective (*e.g.*, a Mitutoyo M Plan Apo 100× objective with an NA = 0.9) can achieve a (vendor-specified) resolution of 300 nm. Pulsing the TEC power causes the local dewdrop to appear and disappear almost instantaneously, which helps reveal otherwise-invisible droplets such as appear in Supporting Movie 2 (Supporting Figure 7). We believe that, by employing methodical lock-in techniques and centroid localization,[30] condensation thermometry might be further developed to achieve a spatial precision of ≲100 nm.

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Setting $T_{chip} < T_c$ causes droplets appear across the substrate surface, but they are not as closely or as uniformly spaced as might be desired (Supporting Movies 3 and 4). A chemical, thermal, or plasma surface treatment likely could be discovered that would result in a dense and optically uniform field of nucleation sites for condensation.[50] Such a field would allow for spatial mapping, and thus condensation thermography, with spatial resolution as discussed above, since the spatial resolution might otherwise be limited by either the nucleation site density or the droplet size (for $T_{chip} < T_c$). For instance, one might set T_{chip} just below T_c to create a field of small droplets, then power the device while observing where and when the droplets disappear. For high spatial precision, detecting cold spots (performed with $T_{chip} > T_c$) is preferred to detecting hot spots (performed with $T_{chip} < T_c$), since locating a single droplet appearing in an empty field is easier than locating a single droplet disappearing in a dense field of droplets.

Not having yet undertaken an investigation of surface treatments, we still find that the dewdrops appearing by chance on the device of Figure 3 are sufficient to roughly locate its hot and cold spots. Pulsing the TEC power causes droplets at the semiconductor junction and the semiconductor-metal junctions to appear and disappear such that the semiconductor junction droplet is (semiconductor-metal junction droplets are) in-phase (out-of-phase) with the TEC power (Supporting Movie 3). In other words, when the TEC is turned on, its center cools (condensing a droplet) while simultaneously its outer contacts heat (evaporating droplets).

CONCLUSIONS

In summary, we have fabricated microscale, electron-transparent TECs from single-crystal flakes of Bi_2Te_3 and $Sb_{2-x}Bi_xTe_3$. Measured with PEET in the high-vacuum environment of a TEM, these devices prove capable of reaching temperatures ∼21 K below ambient, despite an unmitigated heat leak through the supporting Si_3N_4 membrane. Operated in an ambient atmosphere, these devices condense and evaporate droplets of water, which vividly demonstrates their functionality while also providing a spatially resolved temperature signal. This signal serves as the basis for condensation thermometry, a simple, inexpensive, and quantitative technique for mapping temperature changes with ≲300 nm spatial precision.

METHODS

To fabricate electron-transparent TECs, we exfoliate[13,15,16] single crystals of commercially available n-type Bi_2Te_3 and p-type $Sb_{2-x}Bi_xTe_3$ from millimeter-scale cubes (Custom Thermoelectric) onto PDMS films using adhesive tape. The exact stoichiometry is not well-known to us; the vendor only describes the source materials as alloys of "Bi, Te, Se, and Sb along with some dopants." Energy-dispersive X-ray spectroscopy (EDS) indicates stoichiometries of $Bi_{39}Te_{59}Se_2$ and $Sb_{24}Bi_{14}Te_{61}Se_1$, respectively. Suitable flakes, which are 5−10 μm long, 1−4 μm wide, and appear thin, are found in an optical microscope. They are then transferred by dry-stamping of the PDMS (ref 51) to prepared substrates. A substrate consists of a 200 μm thick silicon chip with a central, 20 nm-thick Si_3N_4 window and multiple, bordering 25 nm thick platinum electrodes (with a 5 nm-thick titanium adhesion layer) that have been patterned using optical lithography.[52] Scanning electron microscopy (SEM) and atomic force microscopy (AFM) measurements (see Supporting Information) show that the flakes are typically 20−150 nm (or 7−50 quintuple layers[13]) thick, and TEM diffraction shows that the flakes are single crystals. First an n-type flake, and then a p-type flake, is placed onto the target silicon nitride window such that each overlaps an electrode and, in the center of the window, each other (Figure 1). This geometry, which features predominantly in-plane conduction (the c-axes of the flakes are normal to the chip), is advantageous because the electrical conductivity of bismuth telluride is more strongly anisotropic than the lattice conductivity.[10,40] However, it is disadvantageous in that the supporting Si_3N_4 membrane, which has $\kappa_{SiN} \simeq 2\kappa_{BiTe}$, acts to short any temperature gradient produced by the device. After assembly a device's resistance is measured in the ambient atmosphere. High resistance devices are annealed as described in the main text. Finally, an indium film, nominally 8 nm thick, is deposited on the chip *via* electron beam evaporation, which produces across the entire sample a uniform density of nanoparticles, many of which are ∼50 nm in diameter (Figure 1). Indium is deposited and used as a nanothermometer because, unfortunately, the plasmon peaks of Bi_2Te_3, $Sb_{2-x}Bi_xTe_3$, and Si_3N_4 are too ill-defined to give precise peak energies, and thus are not useful for PEET. With a zero-loss peak (ZLP) fwhm of 0.67 eV, we measure indium's plasmon energy as E_p = 11.1−11.5 eV, with a fwhm of 1.2 eV. The measured E_p value is within 9−13% of the electron-gas-model prediction $\hbar\sqrt{e^2 n/\epsilon_0 m}$, and the linear thermal expansion coefficient is a relatively large 3×10^{-5} K^{-1}. (See discussion of Figure 2 for exact values.) These properties indicate indium's suitability and sensitivity, respectively, as a thermometric material. Because the indium film is discontinuous (Figure 1), its effects on the TEC devices' electrical properties is negligible, and its effects on their thermal properties is expected to be likewise.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.0c03958.

- Captions for the four movies, nine additional figures describing the device architecture and data analysis, and a section detailing procedures for PEET curve fitting (PDF)
- An optical movie of a TEC device condensing a dew drop near the heterojunction (MP4)
- An optical movie of a TEC device condensing a barely visible droplet near the heterojunction (MP4)
- An optical movie of a TEC device demonstrating simultaneous heating and cooling in different regions while under bias (MP4)
- An optical movie of a TEC device condensing a large dew drop over the heterojunction (MP4)

AUTHOR INFORMATION

Corresponding Author

B. C. Regan − *Department of Physics and Astronomy and California NanoSystems Institute, University of California, Los Angeles, California 90095, United States;* orcid.org/0000-0003-3923-2688; Email: regan@physics.ucla.edu

Authors

William A. Hubbard − *Department of Physics and Astronomy and California NanoSystems Institute, University of California, Los Angeles, California 90095, United States;* orcid.org/0000-0002-2924-0820

Matthew Mecklenburg − *Core Center of Excellence in Nano Imaging, University of Southern California, Los Angeles, California 90089, United States;* orcid.org/0000-0003-0581-4153

Jared J. Lodico − *Department of Physics and Astronomy and California NanoSystems Institute, University of California, Los Angeles, California 90095, United States*

Yueyun Chen − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*

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Xin Yi Ling − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
Roshni Patil − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
W. Andrew Kessel − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
Graydon J. K. Flatt − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
Ho Leung Chan − *Department of Physics and Astronomy and California NanoSystems Institute, University of California, Los Angeles, California 90095, United States*
Bozo Vareskic − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
Gurleen Bal − *Department of Physics and Astronomy, University of California, Los Angeles, California 90095, United States*
Brian Zutter − *Department of Physics and Astronomy and California NanoSystems Institute, University of California, Los Angeles, California 90095, United States;* orcid.org/0000-0002-3604-5791

Complete contact information is available at:
https://pubs.acs.org/10.1021/acsnano.0c03958

Author Contributions

[‖]W.A.H., M.M., and J.J.L. contributed equally.

Notes

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